matrix on an entire surface of the wafer except for on scribe lines between the semiconductor chips, each semiconductor chip of said semiconductor chips including:

a first surface upon which said bump electrodes are formed;

[a second surface opposite said first surface;]

a periphery adjacent said scribe lines;

a plurality of chip electrodes formed [on said second surface] between said first surface and said wafer along said periphery; and

a plurality of interconnection layers, each of said interconnection layers including a first end connected to a bump electrode of said bump electrodes and a second end connected to a corresponding chip electrode of said chip electrodes,

each of said bump electrodes being located at a position other than over said corresponding chip electrode.

C1 cont.

~~18.~~ 13. (Amended) A semiconductor wafer [as in claim 10] including:

a plurality of chip sections defined thereon by scribe lines, each chip section having bump electrodes formed simultaneously thereon, the scribe lines for separating the chip sections from each other without dividing bump electrodes thereon, said chip section including:

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum layer, wherein said plating contacts one of said bump electrodes and said aluminum layer contacts one of said chip electrodes.

C2